True Differential,Dual,1 MSPS, 14-Bit/12-Bit, 2-Channel SAR ADC With PGA

Preliminary Technical Data

AD7264/AD7262

FEATURES

Dual Simultaneous sampling 14-bit/12-bit, 2-channel ADC
True Differential Analog Inputs
Programmable Gain Stage:
×1, ×2, ×3, ×4, ×6, ×8, ×12, ×16, ×24, ×32, ×48,× 64, ×96, x128
AD7264 Throughput rate per ADC: 1 MSPS
AD7262 Throughput rate per ADC: 1 MSPS
Analog Input impedance: > 1GΩ
Wide input bandwidth
-3dB bandwidth: > 100 kHz
4 On-chip Comparators
Specified for V_{CC} of 5 V ± 5%
Low current consumption: 24mA
Guaranteed Monotonic
Device offset calibration
System offset and gain calibration
On-chip reference: 2.5 V
–40°C to +105°C operation
High speed serial interface
SPI®/QSPI™/MICROWIRE™/DSP compatible
48-lead TQFP/LFCSP Package

GENERAL DESCRIPTION

The AD7264/AD7262 are dual, 14-bit/12-bit, high speed, low power, successive approximation ADC that operates from a single 5 V power supply and features throughput rates up to 1MSPS, per on-chip ADC. Two Complete ADC Functions Allow Simultaneous Sampling and Conversion of Two Channels. The conversion result of both channels is simultaneously available on separate data lines, or in succession on one data line if only one serial port is available. The device contains two ADCs, each preceded by a true differential analog input with a PGA. There are thirteen gain settings available, ×1, ×2, ×3, ×4, ×6, ×8, ×12, ×16, ×24, ×32, ×48, ×64, ×96 and x128. In addition, the AD7264/AD7262 contains four comparators. Comparators A and B are optimised for low power while comparator C and D have short propagation delays. The AD7264/AD7262 features a calibration function to remove the devices offset error and programmable offset and gain adjust registers to allow for input path (e.g. sensor) offset and gain compensation. The AD7264/AD7262 has an on-chip 2.5 V reference that can be overdriven if an external reference is preferred. The AD7264/AD7262 is available in a 48-lead TQFP or LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

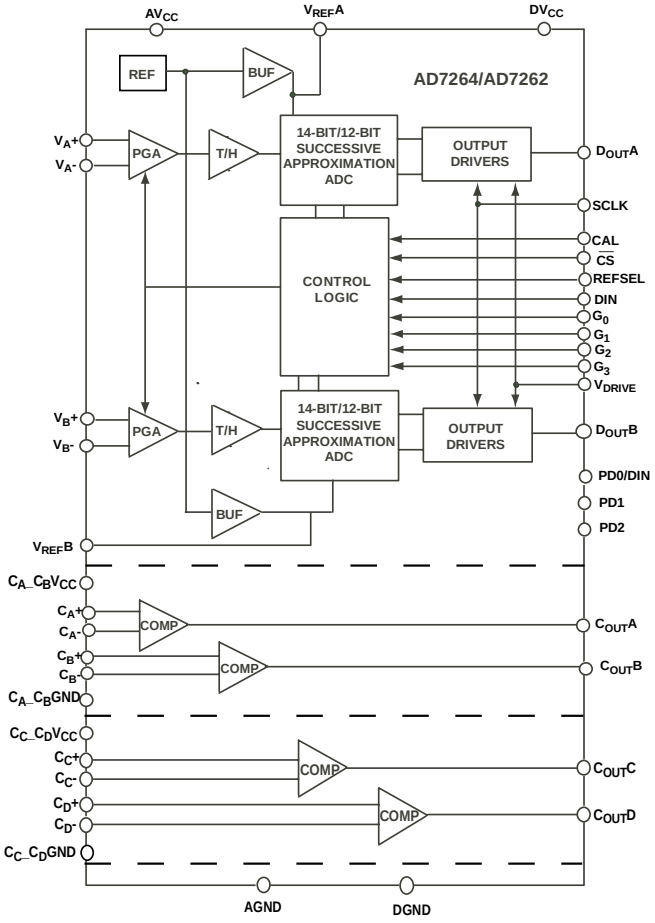

Figure 1

Table 1.Related Products

Device Number	Resolution	Throughput Rate	Number of Channels
AD7264	14-Bit	1 MSPS	Dual, 2-ch
AD7262	12-Bit	1 MSPS	Dual, 2-ch
AD7264-5	14-Bit	500 KSPS	Dual, 2-ch
AD7262-5	12-Bit	500 KSPS	Dual, 2-ch

Rev. PrA

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REVISION HISTORY

09/06—Revision PrE: Initial Version

SPECIFICATIONS FOR AD7264

AV_{CC} = DV_{CC} = 5 V ± 5%, C_A_$C_B V_{CC}$ = C_C_$C_D V_{CC}$ =2.7 V to 5.25V, V_{DRIVE} = 2.7 V to 5.25V, f_{SAMPLE} =1 MSPS, f_{SCLK} = 34MHz, V_{REF} = 2.5 V Internal/External; T_A = T_{MIN} to T_{MAX}, unless otherwise noted[1].

Table 2.

Parameter	Value			Unit	Test Conditions / Comments
	Min	Typ	Max		
DYNAMIC PERFORMANCE					f_{IN} = 100 kHz sine wave;
Signal-to-Noise Ratio (SNR)[2]	78	80		dB	PGA Gain setting = 1
Signal-to-Noise + Distortion Ratio (SINAD) [2]	77			dB	
Total Harmonic Distortion (THD) [2]		-82		dB	
Spurious Free Dynamic Range (SFDR)[2]		-82		dB	
Common Mode Rejection Ratio (CMRR) [2]		<-70		dB	For ripple frequency of 50/60Hz; see Figure x.
Channel-to-Channel Isolation[2]		-88		dB	
Bandwidth		100		kHz	@ -3 dB; PGA gain setting = 128
DC ACCURACY					
Resolution			14	Bits	
Integral Nonlinearity[2]			±2	LSB	
Differential Nonlinearity[2]			±0.99	LSB	Guaranteed no missed codes to 14 bits
Offset Error[2]			±5	LSB	After Calibration
Offset Error Match[2]		±1		LSB	
Offset Drift		5		µV/°C	
Gain Error[2]		±0.1%	TBD	FSR	
Gain Error Match		±0.5		LSB	
ANALOG INPUT					
Input Voltage Range: V_+ and V_-[3]	V_{CM} - V_{REF}/(2xGain)		V_{CM} + V_{REF}/(2xGain)	V	For Gain >1, V_{CM} = AV_{CC}/2
Common mode Voltage, V_{CM}	2.5V- 100mV		2.5V +100mV	V	F
DC Leakage Current			±1	µA	
Input Capacitance		3		pF	
Input Impedance		>1		GΩ	
REFERENCE INPUT/OUTPUT					
Reference Output Voltage[4]	+2.49		+2.51	V	±0.2% max @ 25°C
Reference Input Voltage Range	+2.49		+2.51	V	
DC Leakage Current			±1	µA	External reference applied to Pin V_{REF}A/Pin V_{REF}B
Input Capacitance		25		pF	
V_{REF}A, V_{REF}B Output Impedance		10		Ω	
Reference Temperature Coefficient		20		ppm/°C	
V_{REF} Noise		20		$µV_{RMS}$	
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7× V_{DRIVE}			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}			±1	µA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[4]		5		pF	

LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2			V	
Output Low Voltage, V_{OL}			0.4	V	
Floating State Leakage Current			±1	µA	
Floating State Output Capacitance[4]		10		pF	
Output Coding				Two's Complement	
CONVERSION RATE					
Conversion Time			530	ns	18 × t_{SCLK}, For 4.75V<V_{DRIVE}≤5.25V
Cycle Time			970	ns	33 × t_{SCLK}, For 4.75V<V_{DRIVE}≤5.25V
AC Acquisition Time[4]			440	ns	For 4.75V<V_{DRIVE}≤5.25V
Throughput Rate			1	MSPS	For 4.75V<V_{DRIVE}≤5.25V
		>750	TBD	KSPS	For 2.7V≤V_{DRIVE}≤4.75V
COMPARATORS					
Input Offset range			±4.5	mV	
		±2.5		mV	
Input Common Mode Range		0 to 3.5		V	
Input Impedance		>1		GΩ	
I_{DD} Normal Mode (Static)					No Load, C_{OUT}=0V
Comparator A & B		0.90		µA	C_A_$C_B$$V_{CC}$ = 2.7V
""		1.80		µA	C_A_$C_B$$V_{CC}$ = 5V
Comparator C & D		13		µA	C_C_$C_D$$V_{CC}$ = 2.7V
""		27.0		µA	C_C_$C_D$$V_{CC}$ = 5V
Propagation Delay Time- High to Low					
Comparator A & B		2.30		µs	C_A_$C_B$$V_{CC}$ = 2.7V
""		1.70		µs	C_A_$C_B$$V_{CC}$ = 5V
Comparator C & D		0.20		µs	C_C_$C_D$$V_{CC}$ = 2.7V
""		0.14		µs	C_C_$C_D$$V_{CC}$ = 5V
Propagation Delay Time- Low to High					
Comparator A & B		1.70		µs	C_A_$C_B$$V_{CC}$ = 2.7V
""		0.90		µs	C_A_$C_B$$V_{CC}$ = 5V
Comparator C & D		0.210		µs	C_C_$C_D$$V_{CC}$ = 2.7V
""		0.12		µs	C_C_$C_D$$V_{CC}$ = 5V
POWER REQUIREMENTS					Digital I/Ps = 0 V or V_{DRIVE}
AV_{DD}	4.75		5.25	V	
DV_{DD}	4.75		5.25	V	Throughput Rate = 1Msps
	2.7		4.75	V	Throughput Rate < 1Msps[5]
C_A_$C_B$$V_{CC}$, C_C_$C_D$$V_{CC}$	2.7		5.25	V	
V_{DRIVE}	2.7		5.25	V	
I_{DD}					
Normal Mode (Static)			19	mA	V_{DD} = 5.25 V
Operational			24	mA	f_s = 1MSPS, V_{DD} = 5.25 V
Shut-Down Mode			1	µA	
Power Dissipation					
Normal Mode (Operational)			120	mW	
Shut-Down			5.25	µW	

[1] Temperature range is −40°C to +105°C
[2] See Terminology section.
[3] For Gain =1 the maximum analog input signal is V_{CM} ±1.0V
[4] Refers to pins V_{REF}A or V_{REF}B.
[5] The AD7262 is functional but the performance specified in this specification table does not applies with these conditions.

SPECIFICATIONS FOR AD7262

AV_{CC} = DV_{CC} = 5 V ± 5%, C_A_$C_B V_{CC}$ = C_C_$C_D V_{CC}$ =2.7 V to 5.25V, V_{DRIVE} = 2.7 V to 5.25V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 32MHz, V_{REF} = 2.5 V Internal/External; T_A = T_{MIN} to T_{MAX}, unless otherwise noted[1].

Table 3.

Parameter	Value			Unit	Test Conditions / Comments
	Min	Typ	Max		
DYNAMIC PERFORMANCE					f_{IN} = 100 kHz sine wave;
Signal-to-Noise Ratio (SNR)[2]	69	72		dB	PGA Gain setting = 1
Signal-to-Noise + Distortion Ratio (SINAD) [2]	69			dB	
Total Harmonic Distortion (THD) [2]		-80		dB	
Spurious Free Dynamic Range (SFDR)[2]		-75		dB	
Common Mode Rejection Ratio (CMRR) [2]		<-70		dB	For ripple frequency of 50/60Hz; see Figure x.
Channel-to-Channel Isolation[2]		-88		dB	
Bandwidth		100		kHz	@ -3 dB; PGA gain setting = 128
DC ACCURACY					
Resolution			12	Bits	
Integral Nonlinearity[2]			±1	LSB	
Differential Nonlinearity[2]			±0.99	LSB	Guaranteed no missed codes to 12 bits
Offset Error[2]			±5	LSB	After Calibration
Offset Error Match[2]		±1		LSB	
Offset Drift		5		µV/°C	
Gain Error[2]		±0.1%	TBD	FSR	
Gain Error Match		±0.5		LSB	
ANALOG INPUT					
Input Voltage Range: V_+ and V_-[3]	V_{CM} - V_{REF}/(2xGain)		V_{CM} + V_{REF}/(2xGain)	V	For Gain >1, V_{CM} = AV_{CC}/2
Common mode Voltage, V_{CM}	2.5V- 100mV		2.5V +100mV	V	Common mode Voltage, V_{CM}
DC Leakage Current			±1	µA	
Input Capacitance		3		pF	
Input Impedance		>1		GΩ	
REFERENCE INPUT/OUTPUT					
Reference Output Voltage[4]	+2.49		+2.51	V	±0.2% max @ 25°C
Reference Input Voltage Range	+2.49		+2.51	V	
DC Leakage Current			±1	µA	External reference applied to Pin V_{REF}A/Pin V_{REF}B
Input Capacitance		25		pF	
V_{REF}A, V_{REF}B Output Impedance		10		Ω	
Reference Temperature Coefficient		20		ppm/°C	
V_{REF} Noise		20		$µV_{RMS}$	
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7× V_{DRIVE}			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}			±1	µA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[4]		5		pF	

LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2			V	
Output Low Voltage, V_{OL}			0.4	V	
Floating State Leakage Current			±1	µA	
Floating State Output Capacitance[4]		10		pF	
Output Coding				Two's Complement	
CONVERSION RATE					
Conversion Time			560	ns	$18 \times t_{SCLK}$, For $4.75V<V_{DRIVE}\leq5.25V$
Cycle Time			969	ns	$31 \times t_{SCLK}$, For $4.75V<V_{DRIVE}\leq5.25V$
AC Acquisition Time[4]			440	ns	For $4.75V<V_{DRIVE}\leq5.25V$
Throughput Rate			1	MSPS	For $4.75V<V_{DRIVE}\leq5.25V$
		>750	TBD	KSPS	For $2.7V\leq V_{DRIVE}\leq4.75V$
COMPARATORS					
Input Offset range			±4.5	mV	
		±2.5		mV	
Input Common Mode Range		0 to 3.5		V	
Input Impedance		>1		GΩ	
I_{DD} Normal Mode (Static)					No Load, C_{OUT}=0V
Comparator A & B		0.90		µA	$C_A\_C_BV_{CC}$ = 2.7V
""		1.80		µA	$C_A\_C_BV_{CC}$ = 5V
Comparator C & D		13		µA	$C_C\_C_DV_{CC}$ = 2.7V
""		27.0		µA	$C_C\_C_DV_{CC}$ = 5V
Propagation Delay Time- High to Low					
Comparator A & B		2.30		µs	$C_A\_C_BV_{CC}$ = 2.7V
""		1.70		µs	$C_A\_C_BV_{CC}$ = 5V
Comparator C & D		0.20		µs	$C_C\_C_DV_{CC}$ = 2.7V
""		0.14		µs	$C_C\_C_DV_{CC}$ = 5V
Propagation Delay Time- Low to High					
Comparator A & B		1.70		µs	$C_A\_C_BV_{CC}$ = 2.7V
""		0.90		µs	$C_A\_C_BV_{CC}$ = 5V
Comparator C & D		0.210		µs	$C_C\_C_DV_{CC}$ = 2.7V
""		0.12		µs	$C_C\_C_DV_{CC}$ = 5V
POWER REQUIREMENTS					Digital I/Ps = 0 V or V_{DRIVE}
AV_{DD}	4.75		5.25	V	
DV_{DD}	4.75		5.25	V	Throughput Rate = 1Msps
	2.7		4.75	V	Throughput Rate < 1Msps[5]
$C_A\_C_BV_{CC}$, $C_C\_C_DV_{CC}$	2.7		5.25	V	
V_{DRIVE}	2.7		5.25	V	
I_{DD}					
Normal Mode (Static)			19	mA	V_{DD} = 5.25 V
Operational			24	mA	f_s = 1 MSPS, V_{DD} = 5.25 V
Shut-Down Mode			1	µA	
Power Dissipation					
Normal Mode (Operational)			120	mW	
Shut-Down			5.25	µW	

[1] Temperature range is −40°C to +105°C
[2] See Terminology section.
[3] For Gain =1 the maximum analog input signal is V_{CM} ±1.0V
[4] Refers to pins $V_{REF}A$ or $V_{REF}B$.
[5] The AD7262 is functional but the performance specified in this specification table does not applies with these conditions.

TIMING SPECIFICATIONS

AV_{CC} = DV_{CC} = 5 V ± 5%, C_A_$C_B V_{CC}$ = C_C_$C_D V_{CC}$ =2.7 V to 5.25V, V_{REF} = 2.5 V Internal/External; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX}		Unit	Description
	2.7V≤V_{DRIVE}≤4.75V	4.75V<V_{DRIVE}≤5.25V		
f_{SCLK}	100	100	kHz min	
	TBD	32	MHz max	For AD7262
	TBD	34	MHz max	For AD7264
$t_{CONVERT}$	TBD	18 × t_{SCLK}	ns max	tSCLK = 1/fSCLK
		530	ns max	For AD7264
		560	ns max	For AD7262
t_{Cycle}	33 × t_{SCLK}	33 × t_{SCLK}	ns max	t_{SCLK} = 1/f_{SCLK} For AD7264
		970	ns max	For AD7264
	31 × t_{SCLK}	31 × t_{SCLK}	ns max	t_{SCLK} = 1/f_{SCLK} For AD7262
		969	ns max	For AD7262
t_{QUIET}	30	30	ns min	Minimum time between end of serial read/Bus Relinquish and next falling edge of $\overline{CS}$
t_2	15	15	ns min	$\overline{CS}$ to SCLK setup time,
t_3	15	15	ns max	Delay from 19th SCLK falling edge until DOUTA and DOUTB are three-state disabled
t_4	TBD	25	ns max	Data access time after SCLK falling edge,
t_5	5	5	ns min	SCLK to data valid hold time,
t_6	0.45 t_{SCLK}	0.45 t_{SCLK}	ns min	SCLK high pulse width
t_7	0.45 t_{SCLK}	0.45 t_{SCLK}	ns min	SCLK low pulse width
t_8	30	30	ns min	$\overline{CS}$ rising edge to falling edge pulse width
t_9	15	15	ns max	$\overline{CS}$ rising edge to DOUTA, DOUTB, high impedance / Bus Relinquish
t_{10}	5	5	ns min	SCLK falling edge to DOUTA, DOUTB, high impedance
	35	35	ns max	SCLK falling edge to DOUTA, DOUTB, high impedance
t_{11}	2	2	µs min	Minimum CAL pin high time
t_{12}	2	2	µs min	Minimum time between the CAL pin high and the $\overline{CS}$ falling edge.
t_{13}	4	4	ns min	DIN set-up time prior to SCLK falling edge
t_{14}	2	2	ns min	DIN hold time after SCLK falling edge

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used. See Terminology section and Figure TBD.

[1] The time required for the output to cross 0.4 V or 2.4 V.

ABSOLUTE MAXIMUM RATINGS

Table 5

Parameter	Rating
V_{DRIVE} to DGND	-03V to DV_{CC}
V_{DRIVE} to AGND	-03V to AV_{CC}
AV_{CC} to AGND, DGND	-0.3V to +7V
AV_{CC} to DV_{CC}	DV_{CC} – 0.3V to 7V
DV_{CC} to AV_{CC}	-0.3V to AV_{CC} +0.3V
DV_{CC} to DGND	-0.3V to +7V
C_A_$C_B$$V_{CC}$ to C_A_C_B_GND,	-0.3V to +7V
C_C_$C_D$$V_{CC}$ to C_C_C_D_GND,	-0.3V to +7V
AGND to DGND	-0.3V to +0.3V
C_A_C_B_GND, C_C_C_D_GND to DGND	-0.3V to +0.3V
Analog Input Voltage to AGND	-0.3V to AV_{CC} +0.3V
Digital Input Voltage to DGND	-0.3V to +7V
Digital Output Voltage to GND	-0.3V to V_{DRIVE} +0.3V
V_{REF}A, V_{REF}B input to AGND	-0.3V to AV_{CC} +0.3V
C_{OUT}A, C_{OUT}B, C_{OUT}C, C_{OUT}D to GND	-0.3V to V_{DRIVE} +0.3V
C_A±, C_B±, C_C±, C_D±, to C_A_C_B_GND, C_C_C_D_GND	-0.3V to C_A_$C_B$$V_{CC}$ / C_C_$C_D$$V_{CC}$ +0.3V
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
TQFP Package	
θ_{JA} Thermal Impedance	TBD°C/W
θ_{JC} Thermal Impedance	TBD°C/W
LFCSP Package	
θ_{JA} Thermal Impedance	25.88°C/W
θ_{JC} Thermal Impedance	TBD°C/W
Pb-free Temperature, Soldering	
Reflow	255°C
ESD	TBD kV

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

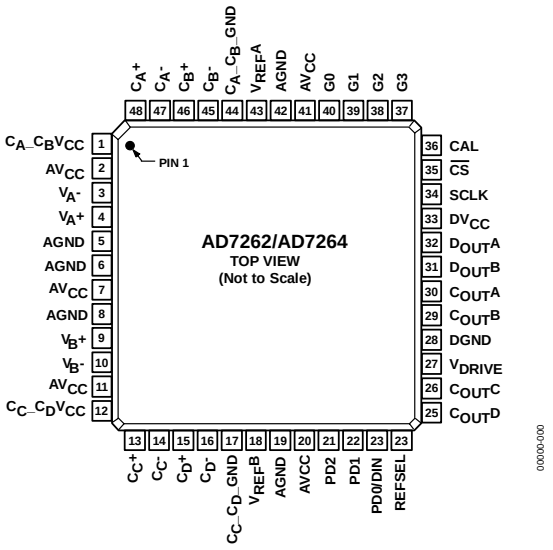


Figure 2: Pin Configuration for TQFP Packager (SU-48)

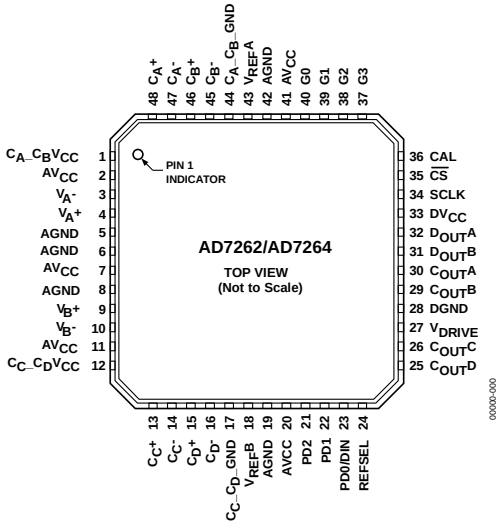


Figure 3: Pin Configuration for LFSCP Package (CP-4)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
2, 7, 11, 20, 41,	AV_{CC}	Analog Supply Voltage, 4.75 V to 5.25 V. This is the supply voltage for the analog circuitry in the AD7264/AD7262. All AV_{CC} pins can be tied together. The AV_{CC} and DV_{CC} voltages should ideally be at the same potential. This supply should be decoupled to AGND.
33	DV_{CC}	Digital Supply Voltage, 2.7V to 5.25 V. This is the supply voltage for the digital circuitry on the AD7264/AD7262. The AV_{CC} and DV_{CC} voltages should ideally be at the same potential, thus these pins can be tied together. Alternatively DV_{CC} can be tied to $V_{DRIVE.}$ For DV_{CC} < 4.75V the throughput rate of the AD7264 and the AD7262 will be less than 1Msps . This supply should be decoupled to DGND.
1	C_A_$C_B V_{CC}$	Comparator Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for comparator A and comparator B. All V_{CC} pins can be tied together. This supply should be decoupled to C_A_C_B_GND.
12	C_C_$C_D V_{CC}$	Comparator Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for comparator C and comparator D. All V_{CC} pins can be tied together. This supply should be decoupled to C_C_C_D_GND.
3, 4	V_{A+}, V_{A-},	Analog Inputs of ADC A. True differential input pair.
9, 10	V_{B+}, V_{B-}	Analog Inputs of ADC B. True differential input pair.
43,18	V_{REF}A, V_{REF}B	Decoupling Capacitor Pins. Decoupling capacitors are connected to these pins to decouple the reference buffer for each respective ADC. Typically, 1µF capacitors are required to decouple the reference. Provided the output is buffered, the on-chip reference can be taken from these pins and applied externally to the rest of a system.
34	SCLK	Serial Clock. Logic input. A serial clock input provides the SCLK for accessing the data from the AD7264/AD7262. This clock is also used as the clock source for the conversion process. A minimum of 33clocks are required to perform the conversion and access the 14-bit result, while 31 clocks are required to access the 12-bit result.
36	CAL	Logic Input. Initiates an internal offset calibration.
21	PD2	Logic input. Places the AD7264/AD7262 in selected shut-down mode in conjunction with PD1 and PD0 pins. See Table 8.
22	PD1	Logic input. Places the AD7264/AD7262 in selected shut-down mode in conjunction with PD2 and PD0 pins. See Table 8.
23	PD0/DIN	Logic input/ Data in. Places the AD7264/AD7262 in selected shut-down mode in conjunction with PD2 and PD0 pins. See Table 8 If all gain selection pins, G_0 – G_3, are tied low, this pin acts as the data input pin and all programming is via the control register see Table 9. Data to be written to the AD7264/AD7262's control register is provided on this input and is clocked into the register on the falling edge of SCLK.

35	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7264/AD7262 and framing the serial data transfer.
48, 47 46, 45	C_A+, C_A-, C_B+, C_B-, -	Comparator inputs. These pin are the inverting and non-inverting analog inputs for comparator A & B. These two comparators have very low power consumption.
13, 14 15, 16	C_C+, C_C-, C_D+, C_D	Comparator inputs. These pin are the inverting and non-inverting analog inputs for comparator C & D. This pair of comparators offers very fast propagation delays.
5, 6, 8, 19, 42,	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7264/AD7262. All analog input signals and any external reference signal should be referred to this AGND voltage. All AGND pins should connect to the AGND plane of a system. The AGND, DGND, C_A_C_B_GND and C_C_C_D_GND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis. C_A_C_B_GND and C_C_C_D_GND can be tied to AGND.
28	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7264/AD7262. Both DGND pins should connect to the DGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
30 29 26 25	C_{OUT}A, C_{OUT}B, C_{OUT}C, C_{OUT}D	Comparator outputs. These pins provide a C-MOS (Push-pull) Output from each respective comparator.
32 31	D_{OUT}A, D_{OUT}B	Serial Data Outputs. The data output from the AD7264/AD7262 is supplied to each pin as a serial data stream in two's complement format. The bits are clocked out on the falling edge of the SCLK input. A total of 33 SCLK's are required to perform the conversion and access the 14-bit data. During the conversion process, the data output pins are in tri-state and once the conversion is finished, the MSB appears. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs. The data is provided MSB first. If $\overline{CS}$ is held low for a further 15 SCLK cycles on either D_{OUT}A or D_{OUT}B following the initial 33 SCLKs, the data from the other ADC follows on the D_{OUT} pin. This allows data from a simultaneous conversion on both ADCs to be gathered in serial format on either D_{OUT}A or D_{OUT}B using only one serial port.
40, 39, 38, 37	G_0 – G_3	Logic Inputs. These are used to program the gain setting of the front-end amplifiers. If all four pins are tied low the pin PD0 acts as a data input pin, DIN and all programming is made via the control register. See Table 7.
27	V_{DRIVE}	Logic Power Supply Input, 2.7 V to 5.25 V. The voltage supplied at this pin determines at what voltage the interface will operate, including the comparator outputs. This pin should be decoupled to DGND.
44, 17	C_A_C_B_GND, C_C_C_D_GND	Comparator Ground. This is the ground reference point for all comparator circuitry on the AD7264/AD7262. Both the C_A_C_B_GND, C_C_C_D_GND pins should connect to the GND plane of a system and can be tied to AGND. The DGND, AGND, C_A_C_B_GND & C_C_C_D_GND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
24	REFSEL	Internal/External Reference Selection. Logic input. If this pin is tied to a logic high voltage, the on-chip 2.5 V reference is used as the reference source for both ADC A and ADC B. In addition, Pin V_{REF}A and Pin V_{REF}B must be tied to 1µF decoupling capacitors. If the REF SELECT pin is tied to GND, an external reference can be supplied to the AD7264/AD7262 through the V_{REF}A and/or V_{REF}B pins. .

TERMINOLOGY

Differential Nonlinearity
Differential nonlinearity is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity
Integral nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a single (1) LSB point below the first code transition and full scale, a point 1 LSB above the last code transition.

Offset Error The deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, that is, AGND + 0.5 LSB.

Gain Error The deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal after adjusting for the offset error, that is, $V_{REF}/2 + V_{CM} - 1.5$ LSB.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio
This ratio is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all non-fundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ \text{dB}$$

Thus for a 14-bit converter, this is 86 dB.

Total Harmonic Distortion (THD)
Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7264/AD7262, it is defined as:

$$THD(dB) = 20\log\frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic, or spurious noise, is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between the ADCA and ADCB. It is measured by applying a full-scale, 100 kHz sine wave signal to all unselected input channels and determining how much that signal is attenuated in the selected channel with a 50 kHz signal. The figure given is the worst-case. See also Typical Performance Characteristics.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum, and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

The AD7264/AD7262 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

PSRR (Power Supply Rejection)
Variations in power supply affect the full-scale transition but not the converter's linearity. Power supply rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value (see figure x).

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7264 and AD7262 are fast, dual, simultaneous sampling, single-supply, differential, 14-bit and 12-bit, Serial A/D converter. The AD7264/AD7262 contains two on-chip differential programmable gain arrays, two track-and-hold amplifiers, two successive approximation A/D converters with a serial interface with two separate data output pins and four on-chip comparators. It is housed in a 48-lead TQFP & LFCSP package, offering the user considerable space-saving advantages over alternative solutions. The AD7264/AD7262 requires a low voltage 5V±5% AV_{CC} & DV_{CC} supply to power the ADC core. The serial clock input accesses data from the part but also provides the clock source for each successive approximation ADC. The AD7264/AD7262 can accept differential analog inputs from VCM -VREF/(2xGain) to VCM +VREF/(2xGain).

The AD7264/AD7262 has an on-chip 2.5 V reference that can be overdriven when an external reference is preferred. If the internal reference is to be used elsewhere in a system, then the output from $V_{REF}A$ & $V_{REF}B$ must first be buffered. On Power up the REFSEL pin must be tied to either a high or low logic state to select either the internal or external reference option. If the internal reference is the preferred option, the user must tie the REFSEL pin logic high. Alternatively, if REFSEL is tied to GND then an external reference can be supplied to both ADC's through $V_{REF}A$ & $V_{REF}B$ pins. (See Reference Section.)

The AD7264/AD7262 also features a range of power-down options to allow the user great flexibility with the independent circuit components while allowing for power saving between conversions. The power-down feature is implemented via the control register or the PD0- PD2 pins as described in the Control Register section.

The on board PGA allows the user to select from 14 programmable gain stages which are x1, x2, x3, x4, x6, x8, x12, x16, x24, x32, x48, x64, x96 & x128. The PGA accepts fully differential analog signal. The gain can be selected by either setting the logic state of pins G_0 to G_3 or by programming the Control Register.

Transfer Function

The AD7264/AD7262 output is two's complement and the ideal transfer characteristic is shown in Figure 4. The designed code transitions occur at successive integer LSB values (i.e. 1 LSB, 2 LSB, and so on). The LSB size is dependant on the analog input range selected.

The LSB size for the AD7264 is

((VCM +VREF/(2xGain)) – (VCM -VREF/(2xGain)))/16384 for Gain >1.

For Gain = 1 & $AV_{CC} \geq 5V$
$((V_{CM}+V_{REF}/2) - (V_{CM}-V_{REF}/2))/16384$.

The LSB size for the AD7262 is

((VCM +VREF/(2xGain)) – (VCM -VREF/(2xGain)))/4096 for Gain >1.

For Gain = 1 & $AV_{CC} \geq 5V$
$((V_{CM}+V_{REF}/2) - (V_{CM}-V_{REF}/2))/4096$.

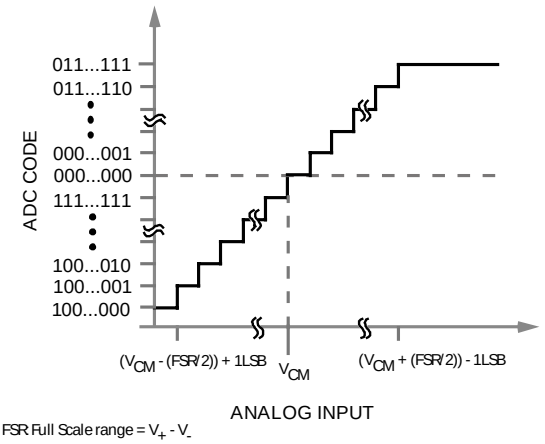


Figure 4. Straight binary transfer function

V_{DRIVE}

The AD7264/AD7264 also has a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, when the AD7264/AD7264 is operated with a AV_{CC} = DV_{CC} =5 V, the V_{DRIVE} pin could be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors. To achieve the maximum throughput rate of 1Msps V_{DRIVE} must be greater than or equal to 4.75V, see table 3. The maximum throughput rate for the AD7264/AD7264 with the V_{DRIVE} voltage set to less than 4.75 and greater than 2.7 is TBD Ksps.

REFERENCE

The AD7264/AD7262 can operate with either the internal 2.5 V on-chip reference or an externally applied reference. The logic state of the REFSEL pin determines whether the internal reference is used. The internal reference is selected for both ADC's when the REFSEL pin is tied to logic high. If the REFSEL pin is tied to GND then an external reference can be supplied through the $V_{REF}A$ and/or $V_{REF}B$ pins. On power-up, the REFSEL pin must be tied to either a low or high logic state for the part to operate. Suitable reference sources for the AD7264/AD7262 include AD780, AD1582, ADR431, REF193, and ADR391.

The internal reference circuitry consists of a 2.5 V band gap reference and a reference buffer. When operating the AD7264/AD7262 in internal reference mode, the 2.5 V internal reference is available at $V_{REF}A$ and $V_{REF}B$ pins, which should be decoupled to AGND using a 1µF capacitor. It is recommended that the internal reference be buffered before applying it elsewhere in the system. The internal reference is capable of sourcing up to TBD µA of current. If the internal reference operation is required for the ADC conversion, the REFSEL pin must be tied to logic high on power-up. The reference buffer requires 700 µs to power up and charge the 1µF decoupling capacitor during the power-up time. The AD7264/AD7262 is specified for a 2.5 V to 3.0 V reference range.

TYPICAL CONNECTION DIAGRAM

Figure 7 & Figure 8 shows a typical connection diagram for the AD7264/AD7262. In this configuration, the AGND pin is connected to the analog ground plane of the system, and the DGND pin is connected to the digital ground plane of the system. The analog inputs on the AD7262/AD7264 are true differential and have an input impedance in excess of 1GΩ hence no driving op-amp are required. The AD7264/AD7262 can operate with either an internal or an external reference. In Figure 7, the AD7264 is configured to operate in control register mode, thus pins G0 – G3, PD1 & PD2 can be connected to ground i.e. low logic state. Figure 8 has the Gain pins configured for a gain of one setup and thus the device is in pin drive mode. Both circuit configurations illustrate the use of the internal 2.5 V reference

The DV_{CC}, $C_A\_C_BV_{CC}$ and the $C_C\_C_DV_{CC}$ pins can be connected to either a 3 V or 5 V supply voltage. The AV_{CC} pin must be connected to a 5V supply. All supplies should be decoupled with a 100nF capacitor at the device pin and some supply sources may require a 10µF capacitor where the source is supplied to the circuit board. The V_{DRIVE} pin is connected to the supply voltage of the microprocessor. The voltage applied to the V_{DRIVE} input controls the voltage of the serial interface V_{DRIVE} can be set to 3V or 5 V.

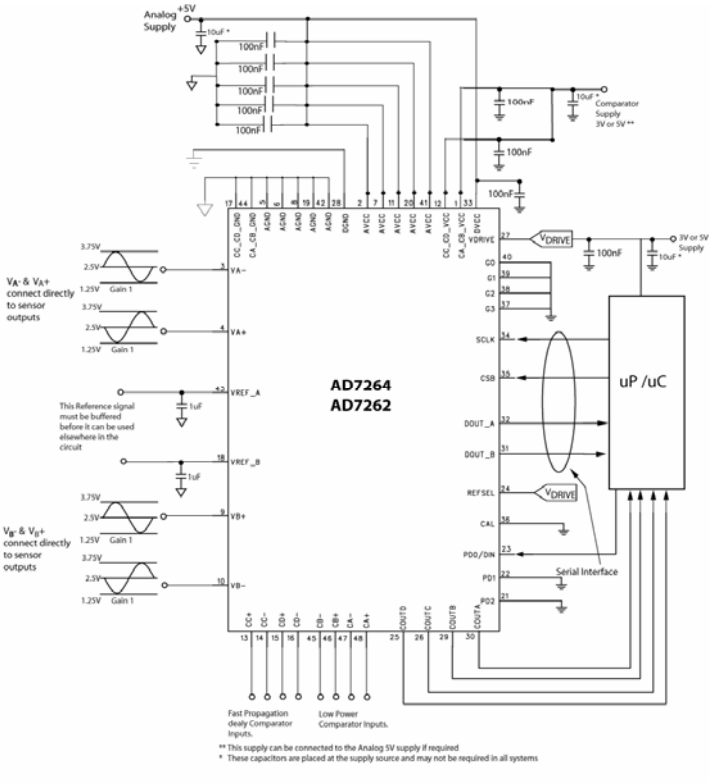


Figure 7. Typical Connection Diagram for the AD7264/AD7262 when in Control Register Mode, thus all Gain pins tied to ground.

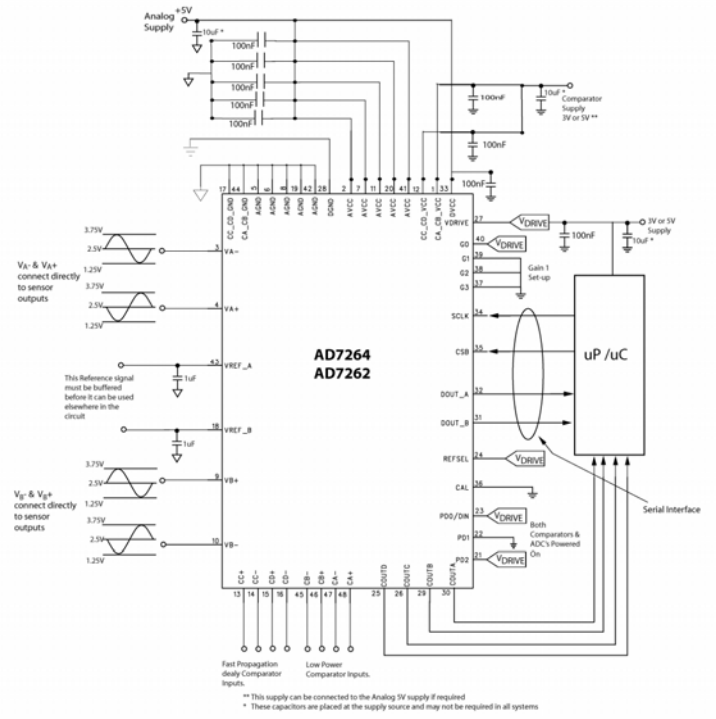


Figure 8. Typical Connection Diagram for the AD7264/AD7262 when in Pin Drive Mode with a Gain of 1 and both ADC's and Comparators fully powered on.

MODES OF OPERATION

The AD7264/AD7262 allows the user to choose between two modes of operation; pin driven mode and control register mode.

PIN DRIVEN MODE

In pin driven mode the user can select the gain of the PGA, the power down mode, internal or external reference and initiating a calibration of the offset for both ADC A and B. These functions are implemented by setting the logic levels on the Gain pins (G3 – G0), power-down pins (PD2 – PD0), REFSEL and the CAL pin respectively.

The logic state of pins G3 to G0 determines which mode of operation is selected. Pin driven mode is selected if at least one of the gain pins is set to a logic high state. Alternatively, if all four Gain pins are connected to a logic low then the Control Register mode of operation is selected.

GAIN SELECTION

The on board PGA allows the user to select from 14 programmable gain stages which are x1, x2, x3, x4, x6, x8, x12, x16, x24, x32, x48, x64, x96 & x128. The PGA accepts fully differential analog signals and provides three key functions, which include selectable gains for small amplitude input signals, drives the ADC's switched capacitive load, and buffers the source from the switching effects of the SAR ADC's. The AD7264/AD7262 offers the user great flexibility in user interface offering gain selection via the control register or by driving the gain pins to the desired logic state. The AD7264/AD7262 has four Gain pins G3, G2, G1 & G0 as illustrated on Figure 2 & Figure 3. Each gain setting is selected by setting up the appropriate logic state on each of the four Gain pins as outlined in Table 7. If all four Gain pins are connected to a logic low level then the gain settings can now be selected via the control register.

Table 7. Gain Selection

G3	G2	G1	G0	Gain
0	0	0	0	Software control via Control Register
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	6
0	1	1	0	8
0	1	1	1	12
1	0	0	0	16
1	0	0	1	24
1	0	1	0	32
1	0	1	1	48
1	1	0	0	64
1	1	0	1	96
1	1	1	0	128

POWER DOWN MODES

The AD7264/AD7262 offers the user a number of power down options to enable individual device components to be powered down independently. These options can be chosen to optimize the power dissipation for different application requirements. The power down modes can be selected by either programming the device via the control register or by driving the PD pins to the appropriate logic levels. By setting the PD pins to a logic low level, when in pin drive mode, all four comparators and both ADC's can be powered down. The PD2 pin must be set to 1 and both the PD1 and PD0 pins set to zero to power up all circuitry on the AD7264/AD7262. The PD pin configurations for the various power-down options are outlined in Table 8.

Table 8. Power Down Modes

PD2	PD1	PD0	Comp A, B	Comp C,D	ADC A,B
0	0	0	OFF	OFF	OFF
0	0	1	OFF	OFF	ON
0	1	0	OFF	ON	OFF
0	1	1	ON	OFF	OFF
1	0	0	ON	ON	OFF
1	0	1	ON	ON	ON
1[1]	1[1]	1[1]	OFF	OFF	OFF

[1] PD2 = PD1 = PD0 = one; resets the AD7262 when in pin drive mode only.

The DV_{CC} and Vdrive supplies must continue to be supplies to the AD7264/AD7262, when the comparators are powered up but the ADC's are in power down. External diodes can be used from the C_A_$C_B V_{CC}$ and/or C_C_$C_D V_{CC}$ to both the DV_{CC} and the V_{DRIVE} supplies to ensure they retain a signal at all instances.

The AD7264/AD7262 can be reset in pin drive mode only by setting the PD pins to a logic high state When the device is reset all the register are cleared and the four comparators and the two ADC are left powered down.

Power up conditions

On power up, the status of the gain pins, determine which mode of operation is selected as outlined in the Gain selection section. All registered are set to zero

If the AD7262/AD7264 is powered up in pin drive mode, the Gain pins and the PD pins should be configuration to the appropriate logic states and a calibration initiated if required.

Alternatively, if the AD7264/AD7262 is powered up in control register mode, the comparators and ADC's are powered down and the default gain is one. Thus, powering up in control register mode requires a write to the device to power up the comparators and the ADC's.

CONTROL REGISTER – SOFTWARE CONTROLLED MODE OF OPERATION

The Control Register on the AD7264/AD762 is a 12-bit, read and write register, which is used to control the device when not in pin drive mode. The PD0/D_{IN} pin serves as the serial D_{IN} pin for the AD7264/AD7262 when the Gain pins are set to zero i.e. the part is not in pin driven mode. The control resister can be used to select the gain of the PGA's, the power down modes and the calibration of the offset for both ADC A and B. When in Control Register mode of operation, PD1 and PD2 should be connected to a low logic state. These functions can also be implemented by setting the logic levels on the Gain pins, power-down pins and the CAL pin respectively. The Control register can also be used to read the internal and external offset and gain registers.

Data is loaded from the PD0/D_{IN} pin of the AD7264/AD7262 on the falling edge of SCLK when $\overline{CS}$ is in a logic low state. The Control Register is selected by first writing the appropriate four WR bits as outlined in Table 11. The 12 data bits must then be clocked into the control register of the device. Thus, on the 16th falling SCLK edge the LSB will be clocked into the device. One more SCLK cycle is then required to write to the internal device registers. In total 17 SCLK cycles are required to successfully write to the AD7264/AD7262. The data is transferred on the PD0/D_{IN} line while the conversion result is being processed. The data transferred on the DIN line corresponds to the AD7264/AD7262 configuration for the next conversion. Only the information provided on the 12 falling clock edges after $\overline{CS}$ falling edge and the initial four address bits is loaded to the Control Register. The PD0/D_{IN} pin should have logic low state for the four bits RD3 to RD0 when using the control register to select the devices power-down modes, gain setting or when initializing a calibration. The RD pin should also be set to a logic low level to access the ADC results from both D_{OUT}A and D_{OUT}B.

The power up status of all bits is zero and the MSB denotes the first bit in the data stream. The bit functions are outlined in Table 9.

Table 9. Control Register Bit Functions

RD3	RD2	RD1	RD0	CAL	PD2	PD1	PD0	G3	G2	G1	G0
MSB											LSB

Table 10. Control Register Bit Function Description

Bit	Mnemonic	Comment
11-8	RD3-RD0	Register address bits. These bits select which register the subsequent read will be from. See Table 12
7	CAL	Setting this bit high initiates an internal offset calibration. Once the calibration is completed this pin can be reset low and the internal offset which is stored in the on-chip offset registers is automatically removed from the ADC's results.
6-4	PD2-PD0	Power-down bits. These bits select which power-down mode is programmed. See Table 8
3-0	G3-G0	Gain selection bits. These bits select which gain setting will be used on the front end PGA. See Table 1

Table 11. Write Address bits

WR3	WR2	WR1	WR0	Read Register Addressed
0	0	0	1	Control register

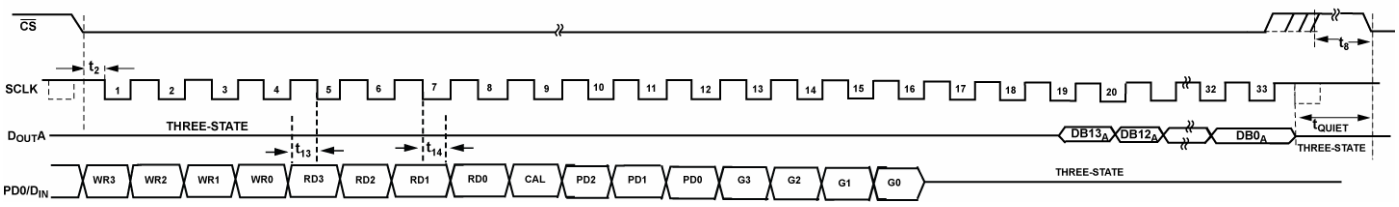


Figure 5. Timing diagram for a write operation to the Control Register.

ON-CHIP REGISTERS

The AD764/62 contains a Control Register, four offset registers for storing both the internal and external offsets for each ADC and two external offset registers. The Control Register, offset and gain registers are read and write registers. The AD7264/AD7262 powers up with all registers set to zero.

Addressing the On-Chip Registers

Writing to a Register

Data is loaded from the PD0/D_{IN} pin of the AD7264/AD7262 on the falling edge of SCLK when $\overline{CS}$ is in a logic low state. Four address bits and 12 data bits must be clocked into the device. Thus, on the 16th falling SCLK edge the LSB will be clocked into the device. One more SCLK cycle is then required to write to the internal device registers. In total 17 SCLK cycles are required to successfully write to the AD7264/AD7262. All registers are 12 bits except the external gain registers, which are 7-bit registers.

When writing to a register one must first write the address bits corresponding to the selected register. The four RD bits are written MSB first, that is RD3 followed by RD2, RD1 & RD0. These bits are decoded by the device to determine which register is being addressed and the subsequent 12 bits of data are written to the addressed register. When writing to the external gain registers, 17 SCLK cycles are still required and the PD0/D_{IN} pin of the AD7264/AD7262 should be tied low for the five additional clocks required. The seven bits of data immediately after the four address bits are written to the register. Table 11 shows the decoding of the address bits.

Table 12. Read & Write register Addresses

RD3	RD2	RD1	RD0	Comment
0	0	0	0	ADC result (default)
0	0	1	0	Offset ADC A Internal
0	0	1	1	Offset ADC B Internal
0	1	0	0	Offset ADC A External
0	1	0	1	Offset ADC B External
0	1	1	0	Gain ADC A External
0	1	1	1	Gain ADC B External

Reading from the Registers

The internal offset of the device, which has been measured by the AD7264/AD7262 and stored in the on-chip registers, can be read back by the user. The content of the external offset and gain registers can also be read. To read the content of any register the user much first write to the control register by writing "0001" for the WR3-WR0 bits via the PD0/D_{IN} pin as outlined in Table 11. The next four bits in the Control Register are the RD pins which are used to select the desired register from which to read. The appropriate four-bit address for each of the offset and gain registers are outlined in Table 12. The remaining eight SCLK cycles bits are used to set the remaining bits in the control register to the desired state for the subsequent ADC conversion. The nineteenth SCLK falling edge will clock out the first data bit of the digital code corresponding to the value stored in the selected internal device register on the D_{OUT}A pin. D_{OUT}B will output the conversion result from ADC B. Once the selected register has been read, the Control Register must be reset to output the ADC results. This is achieved by writing "0001" for the WR3-WR0 bits followed by "0000" for the RD bits. The remaining 8 bits in the Control Register should then be set to the required configuration for the next ADC conversion.

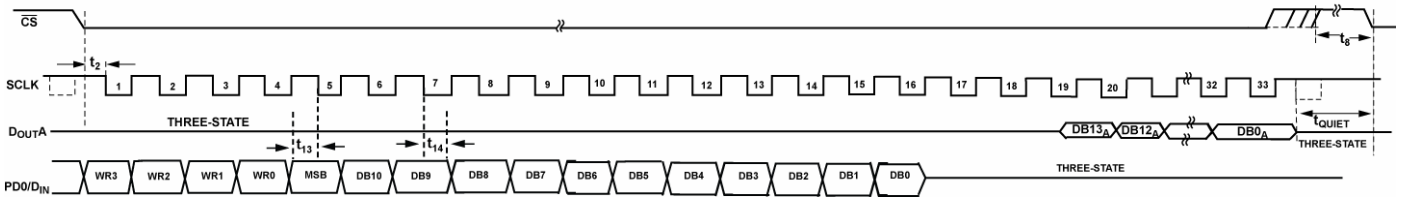


Figure 6. Timing diagram for writing to a register

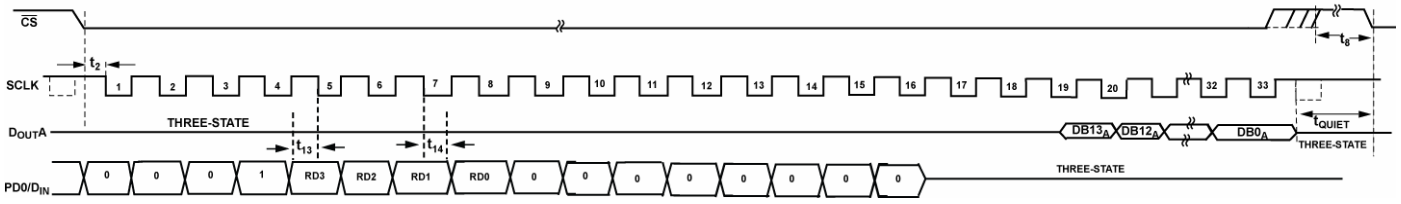


Figure 7. Timing diagram for a read operation with PDO/DIN as an input

SERIAL INTERFACE

Figure 8 and Figure 9 shows the detailed timing diagram for serial interfacing to the AD7264 and AD7262 respectively. The serial clock provides the conversion clock and controls the transfer of information from the AD7264/AD7262 after the conversion. The $\overline{CS}$ signal initiates the conversion process and ensuing data transfer. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, at which point the analog input is sampled and the bus remains in three-state. The conversion is also initiated at this point and requires a minimum of 18 SCLKs to complete and another 14 SCLKs for the AD7264 or 12 SCLK for the AD7262 to clock out the conversion result. On the rising edge of $\overline{CS}$, $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. If $\overline{CS}$ is not brought high (after 33 SCLKs for the AD7264 or 31 SCLK's for the AD7262), but is instead held low for a further 14 SCLK cycles for the AD7264 or 12 SCLK cycles for the AD7262 on $D_{OUT}A$, the data from Conversion B will be output on $D_{OUT}A$. Likewise, if $\overline{CS}$ is held low for a further 14 SCLK cycles for the AD7264 or 12 SCLK cycles for the AD7262 on $D_{OUT}B$, the data from Conversion A will be output on $D_{OUT}B$. This is illustrated in Figure 10 where the case for $D_{OUT}A$ is shown for the AD7264. In this case, the D_{OUT} line in use goes back into three-state on the 47th SCLK falling edge or the rising edge of $\overline{CS}$, whichever occurs first

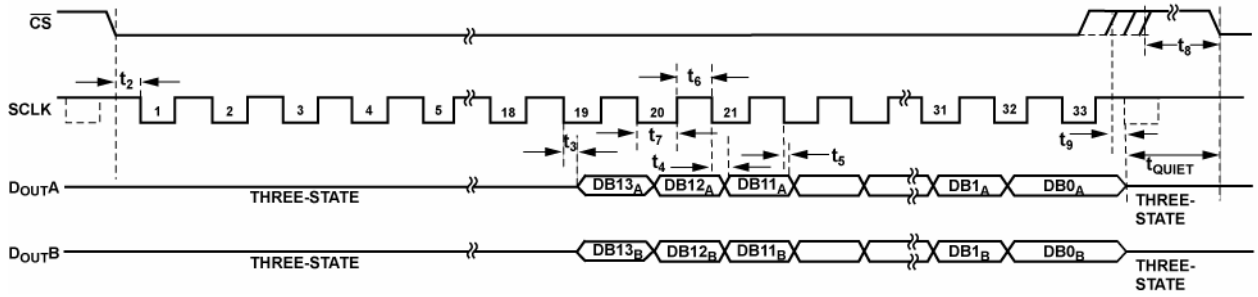


Figure 8 AD7264 Normal Mode Operation

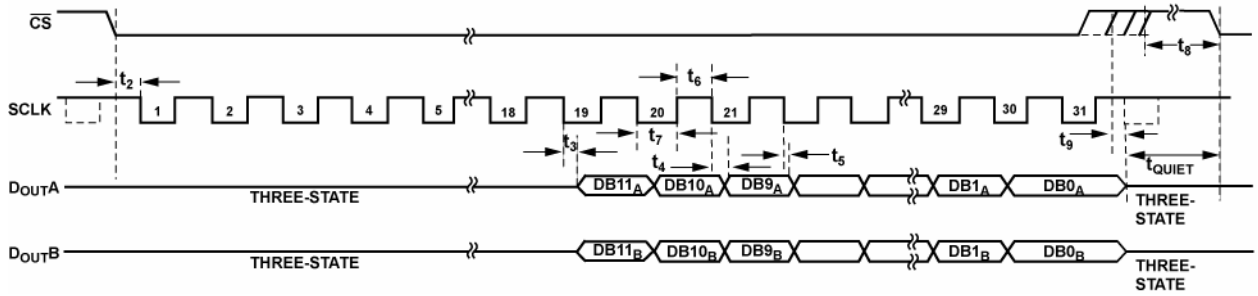


Figure 9 AD7262Normal Mode Operation

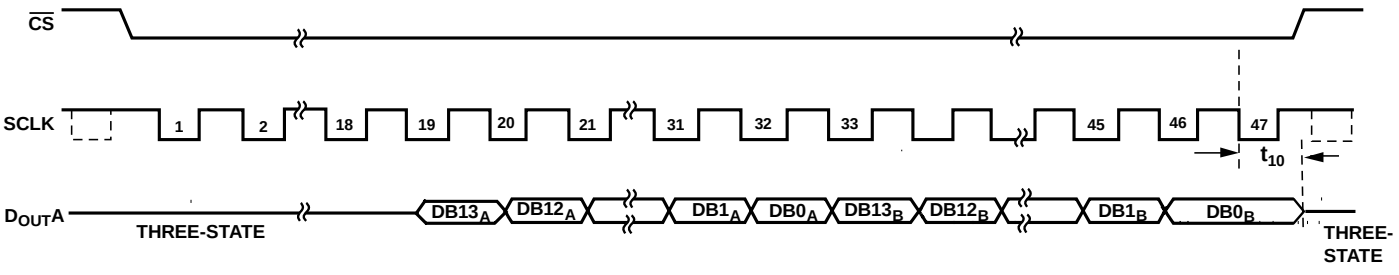


Figure 10 Reading Data from Both ADCs on One D_{OUT} Line with 47 SCLKs for the AD7264

CALIBRATION

Internal Offset Calibration

The AD7264/AD7262 allows the user to calibrate the devices offset using the CAL pin. This is achieved by setting the CAL pin to a high logic level, which initiates a calibration on the next $\overline{CS}$ falling edge. The CAL pin should only be driven high after 19 SCLK cycles have elapse when $\overline{CS}$ is low or when the $\overline{CS}$ pin is high, that is between conversions. The CAL pin must be driven high t_{12} ns before $\overline{CS}$ goes low. If the $\overline{CS}$ pin goes low before the t_{12} has elapsed then the calibration result will be inaccurate for the current conversion but provided the CAL pin remains high the subsequence calibration conversion will be correct. If the CAL pin is set to a logic high state during a conversion, then that conversion result is corrupted. The calibration requires one full conversion cycle, which containing a $\overline{CS}$ falling edge followed by 19 SCLK to complete. The CAL pin should only be driven to a logic low state after the 19th SCLK cycle. Provided the CAL pin has been held high for a minimum of one conversion and that t_{12} & t_{11} have been adhered to the calibration is complete after the 19th SCLK cycle and the CAL can be driven to a logic low state. The CAL pin can remain high for more than one conversion if desired and the AD7264/AD7264 will continue to calibrate. The next $\overline{CS}$ falling edge after the CAL pin has been drive to a low logic state will initiate a conversion of the analog input signal.

Alternatively, one can use the control register to initiate an offset calibration. This is done by setting the CAL bit in the control register to one. The calibration is then initiated on the next $\overline{CS}$ falling edge but the current conversion will be corrupted. The ADC's on the AD7264/AD7262 must remain fully powered-up and 19 SCLK must be provided to the ADC's to complete the internal calibration. The AD7264/AD7262 registers store the offset value where the user can access it, see Reading Registers Section. When the device is calibrating the analog inputs are shorted together internally and a conversion is performed. A digital code representing the offset is stored internally in the offset registers and subsequent conversion results will have this measured offset removed.

When the AD7264/7262 is calibrated the calibration results stored in the internal device registers are only relevant for the particular PGA gain selected at the time of calibration. If the PGA gain is changed then the AD7262/AD7262 must be recalibrated. If the device is not recalibrated when the PGA gain is changed the offset for the previous gain setting will continue to be removed from the digital output code, which may lead to inaccuracies.

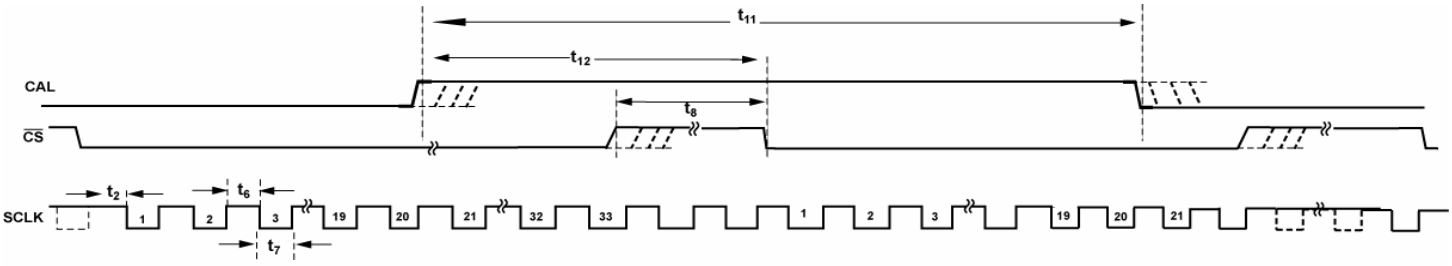


Figure 11 Calibration timing diagram

System Offset and Gain Calibration

The AD7264/AD7264 also allows the user to write to an external offset and gain register, thus enabling the removal of any overall system offset or gain. Both ADC A and ADC B have independent external offset and gain registers allowing the user to calibrate independently the offset and gain on both ADC A's & B's signal paths.

The system calibration function is used by setting the sensors to which the AD7264/AD7262 is connected to a zero offset or gain state. The AD7264/AD7264 converts this analog inputs and the digital output codes, which are available on the D_{OUT} pins, corresponds to the system offset or gain. (depending on whether a zero offset or gain state was inputted to the ADC) This digital output code can then be stored in the appropriate external register. For details on how to write to a register, see the Writing to a Register Section and Table 12.

All the offset and gain registers can be cleared by writing all zeros to each register as outlined in the Writing to a Register Section. In total, the AD7264/AD7262 has six registers for storing both the internal and external offsets and the external gain. Data can be written to or read from all six registers. In self-calibration mode the AD7264/Ad7262 automatically modifies the content of the internal offset registers, only if the user needs to modify the content of these registers should an attempt be made to write to them.

Adjusting the Offset Calibration Registers

Both the external and internal offset calibration register contains 12 bit of data. By changing the contents of the offset register, different amounts of offset on the analog input signal can be compensated for. Increasing the number in the offset calibration register compensates for negative offset on the analog input signal, and decreasing the number in the offset calibration register compensates for positive offset on the analog input signal.

The default value of the internal offset calibration register before any calibration has occurred is all zero's. Each of the 12 data bits in the offset register is binary weighted: the MSB has a weighting of 5% of the reference voltage, the MSB-1 has a weighting of 2.5%, the MSB-2 has a weighting of 1.25%, and so on down to the LSB, which has a weighting of 0.0006%. This gives a resolution of approximately ±0.0006% of V_{REF}. More accurately the resolution is $\pm(0.05 \times V_{REF})/2_{13}$ volts = ±0.015 mV, with a 2.5 V reference. The maximum specified offset that can be compensated for is ±3.75% of the reference voltage but is typically ±5%, which equates to ±125 mV with a 2.5 V reference and ±250 mV with a 5 V reference.

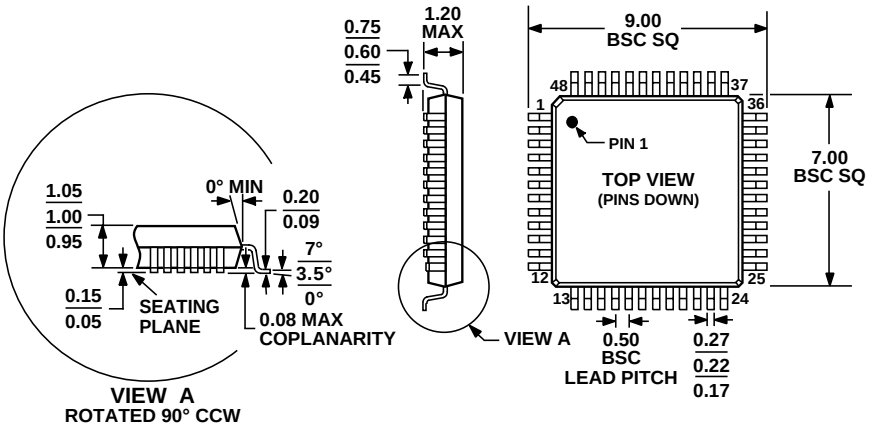
Q. If a +20 mV offset is present in the analog input signal and the reference voltage is 2.5 V, what code needs to be written to the offset register to compensate for the offset?

A. 2.5 V reference implies that the resolution in the offset register is 5% × 2.5 V/2_{13} = 0.015 mV. +20 mV/0.015 mV = 1310.72; rounding to the nearest number gives 1311. In binary terms this is 0101 0001 1111. Therefore, decrease the offset register by 0101 0001 1111.This method of compensating for offset in the analog input signal allows for fine tuning the offset compensation. If the offset on the analog input signal is known, there will be no need to apply the offset voltage to the analog input pins and do a system calibration. The offset compensation can take place in software.

Adjusting the Gain Calibration Registers

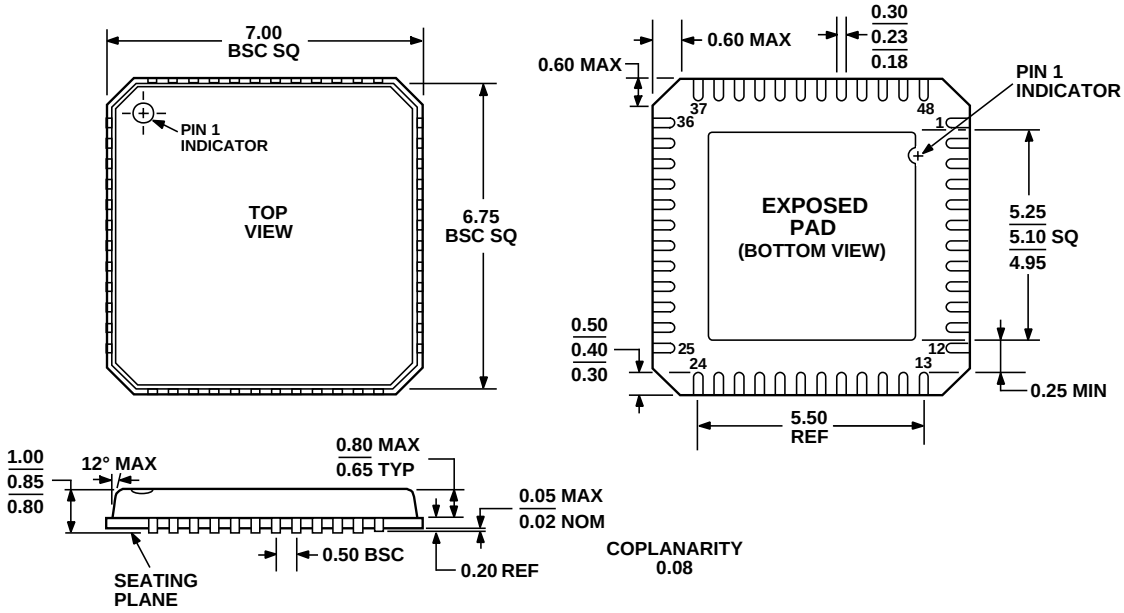
The gain calibration register contains 7 bits of data. The data bits are binary weighted as in the offset calibration register. The gain register value is effectively multiplied by the analog input to scale the conversion result over the full range. Increasing the gain register compensates for a smaller analog input range and decreasing the gain register compensates for a larger input range. The maximum analog input range for which the gain register can compensate is 1.01875 times the reference voltage; the minimum input range is 0.98125 times the reference voltage.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026ABC

Figure 12. 48-Lead TQFP



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 13. 48-Lead LFCSP

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7264BCPZ	−40°C to +105°C	Lead Frame Chip Scale Package	CP-32-3
AD7264BSUZ	−40°C to +105°C	Thin Quad Flat Package	SU-32-2
AD7264BCPZ-5	−40°C to +105°C	Lead Frame Chip Scale Package	CP-32-3
AD7264BSUZ-5	−40°C to +105°C	Thin Quad Flat Package	SU-32-2
AD7262BCPZ	−40°C to +105°C	Lead Frame Chip Scale Package	CP-32-3
AD7262BSUZ	−40°C to +105°C	Thin Quad Flat Package	SU-32-2
AD7262BCPZ-5	−40°C to +105°C	Lead Frame Chip Scale Package	CP-32-3
AD7262BSUZ-5	−40°C to +105°C	Thin Quad Flat Package	SU-32-2

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